

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation structure located in the trench; and

a source/drain region located over the isolation structure.

2. The semiconductor device as recited in Claim 1 wherein

the trench is a first trench and the semiconductor device further

includes a second trench located on an opposing side of the channel

region, wherein the isolation structure is a first isolation

structure located in the first trench and the semiconductor device

further includes a second isolation structure located in the second

trench, and wherein the source/drain region is a first source/drain

region and the semiconductor device further includes a second

source/drain region located over the second isolation structure.

3. The semiconductor device as recited in Claim 1 wherein

the source/drain region comprises polysilicon.

4. The semiconductor devices as recited in Claim 1 wherein

the source/drain region comprises epitaxial silicon.

5. The semiconductor device as recited in Claim 1 wherein a
2 side wall of the trench includes an oxide layer.

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6. The semiconductor device as recited in Claim 5 further
2 including a nitrided layer located on the oxide layer.

7. The semiconductor device as recited in Claim 1 wherein
2 the isolation structure comprises an oxide.

8. The semiconductor device as recited in Claim 1 wherein
2 the source/drain region includes a lightly doped source/drain
3 region having a dopant concentration ranging from about $1E16$
4 atoms/cm³ to about $1E17$ atoms/cm³, and a source/drain contact region
5 having a dopant concentration up to about $1E22$ atoms/cm³.

9. A method of manufacturing a semiconductor device,
2 comprising:

3 forming a channel region in a semiconductor substrate;

4 *Sub 7* forming a trench adjacent a side of the channel region;

5 *A3* forming an isolation structure in the trench; and

6 forming a source/drain region over the isolation structure.

10. The method as recited in Claim 9 wherein forming the
2 trench includes forming a first trench and the method further
3 includes forming a second trench on an opposing side of the channel
4 region, wherein forming the isolation structure includes forming a
5 first isolation structure in the first trench and the method
6 further includes forming a second isolation structure in the second
7 trench, and wherein forming the source/drain region includes
8 forming a first source/drain region and the method further includes
9 forming a second source/drain region over the second isolation
10 structure.

11. The method as recited in Claim 9 wherein forming the
2 source/drain region includes forming a polysilicon source/drain
3 region.

12. The methods as recited in Claim 9 wherein forming the

2 source/drain region includes epitaxially growing the source/drain
3 region from the channel region.

13. The method as recited in Claim 9 further including
2 forming an oxide layer on a side wall of the trench.

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14. The method as recited in Claim 13 further including
2 forming a nitrided layer on the oxide layer.

15. The method as recited in Claim 9 wherein forming an
2 isolation structure includes forming an isolation structure
3 comprising an oxide.

16. The method as recited in Claim 9 wherein forming a
2 source/drain region includes forming a lightly doped source/drain
3 region having a dopant concentration ranging from about $1E16$
4 atoms/cm^3 to about $1E17$ atoms/cm^3 , and forming a source/drain
5 contact region having a dopant concentration up to about $1E22$
6 atoms/cm^3 .

17. An integrated circuit, comprising:

semiconductor devices, including;

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation structure located in the trench; and

a source/drain region located over the isolation structure; and

dielectric layers located over the semiconductor devices and having interconnect structures located therein that electrically connect the semiconductor devices to form an operative-integrated circuit.

18. The integrated circuit as recited in Claim 17 wherein the trench is a first trench and the semiconductor device further includes a second trench located on an opposing side of the channel region, wherein the isolation structure is a first isolation structure located in the first trench and the semiconductor device further includes a second isolation structure located in the second trench, and wherein the source/drain region is a first source/drain region and the semiconductor device further includes a second source/drain region located over the second isolation structure.

19. The integrated circuit as recited in Claim 17 wherein the

2 isolation structure comprises an oxide.

20. The integrated circuit as recited in Claim 17 wherein the
2 semiconductor devices form part of an N-type metal oxide
3 semiconductor (NMOS) device, a P-type metal oxide semiconductor
4 (PMOS) device, a complementary metal oxide semiconductor (CMOS)
5 device, a bipolar device, or a memory device.

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